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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

EX PARTE Chen-Tsai Lee

Application for Patent

Filed: June 21, 2001

Serial No. 09/886,225

FOR:

MEMORY INTERLACE-CHECKING METHOD

(as amended)

APPEAL BRIEF

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Appeal Brief

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I. Real party in interest

The real parties in interest are Chen-Tsai Lee, the inventor named in the subject application, and WINBOND ELECTRONICS CORP., the assignee of record.

II. Related appeals and interferences

There are no related appeals and/or interferences.

III. Status of the claims

A total of 10 claims were presented during prosecution of this application. Claims 5 - 10 have been cancelled. Claims 11-13 have been added. The Applicant appeals the rejected claims 1-4 and 11-13.

IV. Status of amendments

There has been an amendment to the independent claims 4 filed subsequent to the final rejection. The amendment has been entered.

V. Summary of claimed subject matter

The claimed subject matter of the present invention involved in the appeal is directed to a memory interlace-checking method to detect weakened memory in a memory array composed of odd and even addresses. The method comprises sequentially performing accessing commands on the odd/even addresses in the memory array. See pg. 6, line. 1-5. In other words, only a half of memory cells are processed by the read, write or refresh commands, not all memory cells. Further, such actions will induce circuit actions inside the memory and the resultant EMI. The method further comprises sequentially performing data check commands on the even/odd addresses in the memory array that are complementary to the odd/even addresses after the step of performing accessing commands on the odd address.

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See page 6, line 5-10, Figure 1A to Figure 5. Since the data check commands are performed on the even/odd addresses that have been affected by EMI and have not been accessed, the weakened memory elements can be detected. See page 6, ln. 11-15. The claimed matter of the present invention involved in the appeal is also directed to a memory interlace-checking method to detect weakened memory, wherein the method comprises executing a test program, wherein the testing program has at least a portion of main address accessing data, wherein the main address accessing data contains command actions of read, write or refresh in the local addresses. See page 5, ln. 8-10. The method further comprises executing the testing program, wherein the testing program has at least a portion of a secondary address accessing data, which is at least partially complementary to the portion of main address accessing data, wherein the secondary address accessing data contains checking actions that check addresses yet to be triggered by the command actions. See page 5, ln. 13-17.

VI. Grounds of rejection to be reviewed on appeal

Were claims 1-3, 11-13 properly rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of US 4,513,374 to Hooks, Jr. (Hooks hereinafter)?

Was claim 4 properly rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of US 4,513,374 to Hooks, Jr. (Hooks hereinafter)?

VII. Arguments

A. The related law

To establish a prima facie case of obviousness under 35 U.S.C. § 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. Second, there must be suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." MPEP § 2143, 8th ed., February 2003.

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A claimed invention is unpatentable if the differences between it and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C § 103(a); see *Graham v. John Deere Co.*, 383 U.S. 1, 14, 86 S. Ct. 684, 15 L.Ed.2d 545, 148 USPQ 459, 465 (1966).

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

There must be some motivation to combine the references; this motivation must come from "the nature of the problem to be solved, the teachings of the prior art, [or] the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).

"Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blue print for piecing together the prior art to defeat patentability—the essence of hindsight". *In re Dembiczak*, 175 F.3d at 999.

"It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention using the Applicant's structure as a template and selecting elements from the references to fill the gaps". *In re Gorman*, 933 F. 2d 982, 987, 18 USPQ 2d 1885 (Fed. Cir. 1991).

When more than one reference or source of prior art is required in establishing the obviousness rejection, "it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification." *In re Lalu*, 747 F.2d 703, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

"The person of ordinary skill is a hypothetical person who is presumed to be aware of all the pertinent prior art. The actual inventor's skill is not determinative. Factors that may be considered in determining level of skill include : type of problems encountered in art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and education level of active workers in the field." *Customs*

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Accessories Inc. v. Jeffrey-Allan Indus., Inc., 807 F.2d 955, 1 USPQ2d 1196, 1201 (Fed. Cir. 1986).

Finally, if an independent claim is nonobvious under 35 U.S.C. 103 (or unanticipated under 35 U.S.C. 102), then any claim depending therefrom is nonobvious (or unanticipated). *In re Fine*, 837 F.2d 1071, 5 USPQ2d, 1596 (Fed. Cir. 1988).

B. Grouping of the claims

For the first ground of rejection contested by appellant in this appeal, claim 1-3, 11-13 may be treated as one group, and independent claim 1 may be taken as the representative for the issue on appeal. For the second ground of rejection contested by appellant in this appeal, claim 4 may be treated as one group to stand or fall together, and independent claim 4 may be taken as the representative for the issue on appeal.

C. *Claims 1-3, 11-13 were improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted prior art in view of US 4,513,374 to Hooks, Jr. (Hooks hereinafter).*

1. The rejection

In the Office Action mailed on September 8, 2003 (paper No. 3), the Examiner indicated that "the admitted prior art teaches to provide memory interlace check cell by cell in sequence for each row or column, wherein the first step performs command actions on the interlacing memory rows or columns....., inherently including odd/even method of the memory row/column cell testing access". The Examiner further indicated that the Hooks, Jr. teaches to provide the operations in odd/even number manner. The Examiner thus concluded that it would have been obvious to modify the admitted prior art with the teaching of Hooks, Jr. by simply using the odd/even method of the memory cell testing access because one of ordinary skill in the art would use an odd/even memory cell row/column array to provide memory interlace check that may indicate the problem of weakening. See page 6-7 of paper No. 3. In the Office Action mailed on February 27, 2004 (paper No. 5), the Examiner

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indicated that claims 1-6 and 11-13 are unpatentable over the prior art of record by asserting that since Hooks is related to memory systems suitable for use in storing data for image processors, it is conceivable that the address generation approach thereof be of practical use in any memory systems, including test systems for such memory. See page 3 of paper 5. The Examiner further asserted that "absent the positive explicit recitation of testing steps in claims at bar, said claims are not distinguished over the prior art of record".

2. The prior art

The admitted prior art teaches that the conventional memory testing method uses assessing commands (read, write or refresh commands) to test the memory cells **one bit by one bit continuously**. As disclosed by the admitted prior art, the address accessing is performed on, for example as illustrated in Figure 6A, from left to right and then from top to bottom. The continuous accessing scheme as taught by the admitted prior art can not effectively detect memory weakening problems since after finishing the access of the first row and starting the access of the second row, the second row may be strengthened from a weakened state to a normal state due to the assessing commands of write-in, read or refresh applied on the second row.

With references to the prior art Hooks, Hooks is directed to improve image generating process by a memory system. Hooks teaches inputting a signal into the monitor in the interlaced mode for clarity of viewing, and the signal stored in the non-interlaced mode in the frame buffer memory is converted to an interlaced mode by being read out interlaced mode (col. 20, lines 30 et seq.).

3. The prior art differentiated

What significantly distinguishes the method of this invention from the admitted prior art is that the present invention teaches providing accessing commands to the odd/even addresses in the memory array first. Then, data checking commands are provided to the even/odd addresses that are complementary to the odd addresses. In other words, , not all memory cells are processed by read, write or refresh commands, only a half of the memory cells is processed first. In a following step, the data checking commands are the performed on the rest of the memory cells, for example, the even addresses that are yet to be assessed.

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Therefore, the yet to be accesses memory addresses that are weakened by the EMI induced from the previously mentioned command actions can be detected.

The admitted prior art, on the other hand, teaches providing a continuous address commands to all memory cells one bit by one bit, for example, from left/right to right/left, and then row after row.

With respect to the prior art Hook, Hook teaches improving image generating process by use of a memory system in storing data for image processor. Although Hook teaches inputting an image signal in an interlaced mode, there is no where in Hook that either explicitly teaches or implicitly suggests performing accessing commands on the odd addresses and then performing data checking commands on the even addresses. In summary, the memory system of Hook is not directed to a "memory testing" technique and is questionable for a person skilled in the art of memory testing to apply the memory system of Hook to find a solution for overcoming the problems of memory test.

Applicants respectfully submit that in determining the relevant art of the claims in question, one should look to the nature of the problem confronting the present inventor. As stated by the Court in *re Diversitech Corp. Cs. Century Steps, Inc.*, 850 F. 2d 675, 679, 7 USPQ 2d 1315 (Fed. Cir. 1988), **"the problem confronted by the inventor must be considered in determining whether it would have been obvious to combine references in order to solve that problem"**. The problem to be solved by the present invention is to detect weakened memory, while the problem to be solved by Hook is to improve image generating process. Although the Examiner asserted that suggestion or motivation may be found not only in the references but also in the knowledge generally available to one of ordinary skill in the art, the "one of ordinary skill in the art" in this case should be in the art of memory testing. When determining the level of ordinary skill, the Federal Circuit has commented in *Customs Accessories Inc. v. Jeffrey-Allan Indus., Inc.*, that type of problems encountered in the art, prior art solutions to those problems, etc. are factors to be considered. For one skilled in the art of memory testing, one will not be inspired by the solutions of improving image generating process by inputting an image signal in an interlaced mode to propose a solution for memory checking by applying accessing commands to a first group of the memory address followed by applying the data checking commands to a second group of the memory address as specifically taught by the present invention. Applicants further note

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that it is inappropriate hindsight to look back through Applicants' disclosure and declare claim limitation obvious where such declaration can only be guided by Applicants disclosure.

4. Even if combining Admitted prior art and Hook

Applicants respectfully submit that there is no motivation to combine the Admitted prior art with Hook. However, even if there were motivation to modify the method of the Admitted prior art by the odd/even image inputting method, the combination would result with a memory test that provides performing an address accessing on the odd addresses and then performing an address accessing on the even addresses. Therefore, even if the Admitted prior art were combined with Hook, the combination still can not possibly render the memory interlace-checking method of the claimed invention obvious.

D. *Claim 4 was improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted prior art in view US 4,513,374 to Hooks, Jr. (Hooks hereinafter).*

1. The rejection

Claim 4 has been rejected under 35 USC §103(a) as being unpatentable over Hook. The Examiner asserted in paper No. 5 that no testing step method is recited as a limitation in any Claims 1-6 and 11-13. The Examiner also asserted that the Admitted prior art show structures requiring equivalent programming language for testing thereof via computer means. The Examiner further argues there is motivation to combine Admitted prior art with Hook because suggestion or motivation may also in the knowledge generally available to one of ordinary skill in the art.

2. The prior art

The admitted prior art teaches that the conventional memory testing method uses assessing commands (read, write or refresh commands) to test the memory cells **one bit by one bit continuously**. As disclosed by the admitted prior art, the address accessing is performed on, for example as illustrated in Figure 6A, from left to right and then from top to bottom. The continuous accessing scheme as taught by the admitted prior art can not

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effectively detect memory weakening problems since after finishing the access of the first row and starting the access of the second row, the second row may be strengthened from a weakened state to a normal state due to the assessing commands of write-in, read or refresh applied on the second row.

With references to the prior art Hooks, Hooks is directed to improve image generating process by a memory system. Hooks basically teaches inputting a signal into the monitor in the interlaced mode for clarity of viewing, and the signal stored in the non-interlaced mode in the frame buffer memory is converted to an interlaced mode by being read out interlaced mode (col. 20, lines 30 et seq.).

3. The prior art differentiated

What significantly distinguishes the structure of this invention from the admitted prior art reference is that the present invention teaches executing a test program, wherein the test program includes a portion of main address accessing data that contains command actions to provide accessing commands of write, read or refresh command in local addresses in the memory. Afterwards, the test program which also includes a portion of secondary address accessing data containing checking action to provide data checking commands to check addresses yet to be triggered by the accessing command actions. Therefore, the yet to be accessed memory addresses that may be weakened by the EMI induced from the previously mentioned access command actions can be detected.

The admitted prior art, on the other hand, teaches providing a continuous address commands to all memory cells one bit by one bit, for example, from left/right to right/left, and then row after row.

With respect to the prior art Hook, Hook teaches improving image generating process by use of a memory system in storing data for image processor. Although Hook teaches inputting an image signal in an interlaced mode, there is no where in Hook that either explicitly teaches or implicitly suggests performing accessing commands on the odd addresses and then performing data checking commands on the even addresses. In summary, the memory system of Hook is not directed to a "memory testing" technique and is questionable for a person skilled in the art of memory testing to apply the memory system of Hook to find a solution for overcoming the problems of memory test.

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Applicants respectfully submit that in determining the relevant art of the claims in question, one should look to the nature of the problem confronting the present inventor. As stated by the Court in *re Diversitech Corp. Vs. Century Steps, Inc.*, 850 F. 2d 675, 679, 7 USPQ 2d 1315 (Fed. Cir. 1988), "the problem confronted by the inventor must be considered in determining whether it would have been obvious to combine references in order to solve that problem". The problem to be solved by the present invention is to detect weakened memory, while the problem to be solved by Hook is to improve image generating process. Although the Examiner asserted that suggestion or motivation may be found not only in the references but also in the knowledge generally available to one of ordinary skill in the art, the "one of ordinary skill in the art" in this case should be in the art of memory testing. When determining the level of ordinary skill, the Federal Circuit has commented in *Customs Accessories Inc. v. Jeffrey-Allan Indus., Inc.*, that type of problems encountered in the art, prior art solutions to those problems, etc. are factors to be considered. For one skilled in the art of memory testing, one will not be inspired by the solutions of improving image generating process by inputting an image signal in an interlaced mode to propose a solution for memory checking by applying accessing commands to a first group of the memory address followed by applying the data checking commands to a second group of the memory address as specifically taught by the present invention. Applicants further note that it is inappropriate hindsight to look back through Applicants' disclosure and declare claim limitation obvious where such declaration can only be guided by Applicants disclosure.

4. Even if combining Admitted prior art and Hook

Applicants respectfully submit that there is no motivation to combine the Admitted prior art with Hook. However, even if there were motivation to modify the method of the Admitted prior art by the odd/even image inputting method, the combination would result with a memory test that provides performing an address accessing on the odd addresses and then performing an address accessing on the even addresses. Therefore, even if the Admitted prior art were combined with Hook, the combination still can not possibly render the memory interlace-checking method of the claimed invention obvious.

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E. Conclusion

As noted, the Examiner has not properly applied 35 U.S.C. § 102 and U.S.C. § 103 in his rejections of the claims at issue. Accordingly, Applicants believe that the rejections under 35 U.S.C. § 102 and U.S.C. § 103 to be in error, and respectfully request the Board of Appeals and interferences to reverse the Examiner's rejections of the claims on appeal.

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

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VIII. Claims appendix

CLAIMS ON APPEAL:

1. (previously presented) A memory interlace-checking method to detect weakened memory in a memory array composed of odd and even addresses, the method comprising:

sequentially performing accessing commands on the odd addresses in the memory array; and

sequentially performing data checking commands on the even addresses in the memory array that are complementary to the odd addresses.

2. (previously presented) The method of claim 1, wherein the odd and even addresses are memory rows.

3. (previously presented) The method of claim 1, wherein the odd and even addresses are memory columns.

4. A memory interlace-checking method to detect weakened memory, the method comprising:

executing a test program, wherein the testing program has:

at least a portion of main address accessing data, wherein the main address accessing data contains command actions; and

at least a portion of secondary address accessing data, which is at least partially complementary to the portion of main address accessing data, wherein the secondary address accessing data contains checking actions.

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Claims 5-10 (cancelled)

11. (previously presented) A memory interlace-checking method to detect weakened memory in a memory array composed of odd and even addresses, the method comprising:

sequentially performing accessing commands on the even addresses in the memory array; and

sequentially performing data checking commands on the odd addresses in the memory array that are complementary to the odd addresses.

12. (previously presented) The method of claim 1, wherein the odd and even addresses are memory rows.

13. (previously presented) The method of claim 1, wherein the odd and even addresses are memory columns.

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IX. Evidence appendix

There is no evidence submitted pursuant to §§ 1.130, 1.131, or 1.132 of this title or of any other evidence entered by the examiner and relied upon by appellant in the appeal, along with a statement setting forth where in the record that evidence was entered in the record by the examiner.

X. Related proceedings appendix

There are no decisions rendered by a court or the Board in the proceeding identified in the Related Appeals and Interferences section of the brief.